Serial Number: 10/010524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Page 7

Dkt: 884.607US1 (INTEL)

Assignee: Intel Corporation

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 14, 2003, and the references cited therewith.

Claims 1, 9, 12, 15, 18, 23, and 26 are amended; as a result, claims 1-30 remain pending in this application. The claim amendments are consistent with the original filed specification and Applicants do not believe that the amendments introduce any new matter. Correspondingly, entry of these amendments is appropriate.

§102 Rejection of the Claims

Claims 1, 3-9 and 11 were rejected under 35 USC § 102(b) as being anticipated by Greene et al. (U.S. 5,670,993). It is of course fundamental that in order to sustain an anticipation rejection that each and every step or element in the rejected claims must be taught or disclosed in the cited reference. Applicants' respectfully assert that Greene, inter alia, fails to teach or disclose a region as recited in Applicants' amended independent claims 1 and 9.

More specifically, Greene is directed toward techniques for more efficiently performing a complete display screen refresh operation. Greene achieves this by maintaining a redundant memory of pixel data for a display screen, where the redundant memory includes an additional bit flag for each row of pixels defined in the redundant memory. That bit flag is used for purposes of indicating whether any particular row of pixel data is identical to a preceding row or different from a preceding row. *E.g.*, Greene, col. 4, lines 43-50. The purposes of the bit flags are for permitting a screen refresh operation to process a single read from the redundant memory for multiple pixel rows identified in the redundant memory, thereby increasing the processing throughput with which a full screen refresh operation can be performed.

Conversely, Applicants' invention is directed to a selective or sparse refresh operation of a display screen and not a full screen refresh which has been conventionally required and is required and taught, albeit in a different manner, in Greene. This is most notably discernable from Applicants' use of a pixel region. This region is a cluster of pixels that are defined in a frame buffer. Amended claims 1 and 9 recite that this region spans more than one row of pixels. Conversely, Greene organizes or addresses pixels by individual pixel rows.

Serial Number: 10/010524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Page 8

Dkt: 884.607US1 (INTEL)

Assignee: Intel Corporation

Greene's entire teachings hinges on its unique use of a bit flag for a row of pixel data. The addressable units defined in Greene must be organized within a single row to do otherwise would require a complete re-architecture or re-design of Greene. Greene relies on the fact that some rows of pixels are identical to others if a single addressable unit spans more than one row, then Greene would need additional data structures and logic to determine how many rows a single addressable unit spans and whether a next addressable unit is of the same number of rows. Such an ordering of addressable units cannot be achieved within the present confines of the Greene teachings.

Additionally, with respect to Applicants' independent claim 1, Greene does not teach "determining whether the region is the same as a last-modified region," as is recited in Applicants' independent claim 1. Greene determines whether a previous pixel row of its redundant screen display memory is identical to an immediate preceding row, but Greene makes no determination if a row or preceding row was last modified. This makes sense because Greene is not directed to performing a sparse or selective refresh, Greene is directed to performing a complete screen refresh as has been conventionally the case and because of this Greene is not dynamically updating the screen as changes are made; rather, Greene does a complete refresh. Conversely, Applicants' invention dynamically changes the screen display and as a result a determination needs to be made to detect if changes are still occurring to a same region that is being updated to a screen display. This fact is more clearly apparent with respect to Applicants' dependent claim 3.

Accordingly, Applicants respectfully assert that Greene fails to teach a region that is defined and used in the manners recited in Applicants' independent claims 1 and 9. Correspondingly, Applicants respectfully request that the rejections with respect to claims 1, 3-9, and 11 be withdrawn and that these claims be allowed.

§103 Rejection of the Claims

Claims 2, 10, 12, 15-17 and 26-30 were rejected under 35 USC § 103(a) as being unpatentable over Greene et al. in view of Perego (U.S. 5,835,082). When two or more references are combined to assert an obviousness rejection, the proposed combination must be compatible with the purposes and teachings of the individual references that were combined and

Serial Number: 10/010524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Page 9

Dkt: 884.607US1 (INTEL)

Assignee: Intel Corporation

there must be motivation by one of ordinary skill in the art to combine the references. Moreover, in order to sustain an obviousness rejection each and every element or step in the rejected claims must be taught or suggested in the cited references. Applicants assert that Greene and Perego cannot be combined without running contrary to the teachings of Greene, and Applicants assert that any such combination still fails to teach regions and the uses of regions as recited in Applicants' amended independent claims 12, 15, and 26.

At the outset, Applicants would like to point out that claims 2 and 10 are dependent claims from independent claims 1 and 9, respectively. Correspondingly, Applicants assert that based on the arguments presented above with respect to claims 1 and 9 that claims 2 and 10 should be allowed and Applicants respectfully request an indication of the same.

Applicants assert that Greene and Perego cannot be combined to render Applicants' independent claims 12 and 15 obvious because such a combination cannot be supported by the teachings of Greene or Perego and would not be motivated by one or ordinary skill in the art. Both Greene and Perego are directed to limiting the processing throughput associated with performing a screen display refresh and both use two very distinct and different approaches in achieving the same. Greene reduces reads from redundant memory by including an extra bit with each row of addressable units to indicate whether preceding rows are different. Perego reduces reads by introducing another buffer referred to as a compressed frame buffer, which houses unchanged raster lines from a previous refresh. *E.g.*, Perego, col. 3, lines 29-39 and 59-66.

Both Perego and Greene require modifications to the redundant memory or buffers. Both Perego and Greene are directed towards full refreshes and not selective or sparse refresh as in Applicants' invention. Moreover, both Perego and Green add additional structures to the pixel data that is housed in memory or the buffers. Greene includes a redundancy bit and Perego includes a dirty bit to indicate whether the raster line was changed since a last refresh, if no change has occurred than Perego fetches the raster line from the compressed frame buffer and not from the full frame buffer. Combining two different approaches together as a combined data structure with multiple processing techniques for each row of pixel data will result in more processing throughput to refresh a display screen than if a traditional approach was used. This is so, because with such a combination more memory is consumed and more processing logic must

Serial Number: 10/010524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Dkt: 884.607US1 (INTEL)

Assignee: Intel Corporation

be executed, such as logic to reduce retrieval of redundant pixel rows and logic to determine if changes occurred and to decompress any rows that were not unchanged from a compressed frame buffer. It is not likely that one of ordinary skill in the art would take such an approach; since each approach is different and when combined the proposed combination negates the benefits of one approach that is used in isolation. Accordingly, Applicants assert that Greene and Perego cannot be combined and there is no motivation within the art to combine them.

Additionally, Applicants' amended independent claims recite and use "regions" that "span more than one row of pixels." Both Greene and Perego do not define or process pixel data in "regions" as defined in Applicants' invention. That is, neither Green nor Perego are capable of processing pixel blocks that span more than one row and if such an arrangement were used substantial redesign of each of these references would be necessary.

As a result, Applicants respectfully request that the Examiner remove the rejections with respect to claims 2, 10, 12, 15-17, and 26-30.

Claims 13-14 and 18-22 were rejected under 35 USC § 103(a) as being unpatentable over Greene et al. in view of Perego and Tsutsumi (U.S. 5,333,016). Again, in order to sustain an obviousness rejection the proposed combination must teach each and every element or step of the rejected claims, there must be motivation for the proposed combination, and the proposed combination must be compatible with the individual teachings of each of the references.

Claims 13-14 are dependent from independent claim 12 and for the reasons stated above with respect to claim 12, Applicants assert that claim 12 is in condition for allowance.

Correspondingly, claims 13-14 are also in condition for allowance.

Applicants, again assert that there is no motivation from one of ordinary skill in the art to combine Greene with Perego, and as a result the proposed combination of Greene, Perego, and Tsutsumi is asserted to be improper, since such a combination includes the Greene and Perego sub combination.

With respect to amended independent claim 18, the Examiner relies again on the pixel row chunk of processing data that is used in Greene and Perego as a "region" that is recited in Applicants' amended independent claim 18. Applicants have amended independent claim 18, such that a "region spans more than one row of pixels." The combination of Green, Perego, and

Serial Number: 10/010524

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Page 11

Dkt: 884.607US1 (INTEL)

Assignee: Intel Corporation

Tsutsumi does not teach such a "region." Moreover the proposed combination is not capable of processing such a "region" without substantial redesign.

Thus, Applicants assert that the combination fails to teach each and every aspect of Applicants' amended independent claim 18. Accordingly, the rejections with respect to claims 13-14 and 18-22 should be withdrawn and these claims allowed.

Claim 23 was rejected under 35 USC § 103(a) as being unpatentable over Greene et al. in view of Perego and Thacker et al. (U.S. 5,276,851). An obviousness rejection requires that the stated combination teach each and every element of the reject claim and that there be a motivation to combine the cited references. Once again, Applicants assert that Examiner relies on Green for teaching a "region"; however, Applicants' amended independent claim 23 recites a region "that spans more than one row of pixels." For the reasons stated herein and above; Green, Perego, and Thacker fail to teach such a region in combination or in isolation. Once more the proposed combination cannot be made with such a "region" without requiring substantial redesign.

Therefore, Applicants respectfully request that the rejection with respect to claim 23 should be withdrawn and that this claim allowed.

Claim 24 was rejected under 35 USC § 103(a) as being unpatentable over Greene et al. in view of Perego, Thacker et al. and Tsutsumi. Claim 24 is dependent from independent claim 23. Therefore for the reasons stated above, with respect to claim 23, the rejection with respect to claim 24 should be withdrawn and this claim allowed.

Claim 25 was rejected under 35 USC § 103(a) as being unpatentable over Greene et al. in view of Perego, Thacker et al., Tsutsumi and Bell (U.S. 4,958,378). Claim 25 is also dependent from independent claim 23. Thus, for the reasons stated above, with respect to claim 23, the rejection with respect to claim 25 should be withdrawn and this claim allowed.

Serial Number: 10/010524

Assignee: Intel Corporation

Filing Date: December 7, 2001

Title: ENABLING SPARSE REFRESH TECHNIQUES WITH CACHE-LIKE STRUCTURES THAT SNOOP FRAME BUFFER WRITES

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

THOMAS E. WILLIS ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation P.O. Box 2938
Minneapolis, Minnesota 55402

Page 12

Dkt: 884.607US1 (INTEL)

(612) 349-9592

Date 100. 14 2003 By (Inn)

me M. Richards

Ann M. McCrackir

Reg. No. 42,858

Name

Signature